ABSTRACT OF THE DISCLOSURE

A PLL circuit that optimally generates a clock signal with two reference signals having different frequencies. The PLL circuit includes a VCO for generating the clock signal in accordance with a control voltage. A first loop controls the frequency of the clock signal in accordance with a first reference signal. A second loop controls the phase of the clock signal in accordance with a second reference signal, whose cycle is longer than that of the first reference signal. The second loop supplies the VCO with the control voltage at a constant value until the difference between the frequencies of the first reference and clock signals converges to within a predetermined range. Then, the second loop supplies the VCO with a control voltage at a level corresponding to the difference between the phases of the second reference and clock signals.